PHILIP D. GERAMIAN

NORTHBOROUGH, MA | 646-812-1762 | PDGERAMIAN@GMAIL.COM

Skills

ATPG, DFT, BIST, Verilog, VHDL, Tcl, Perl, Python, C/C++, Siemens Tessent, Synopsys VCS, Synopsys Fusion Compiler, Synopsys SpyGlass DFT, Cadence Modus, Cadence Xcelium, Cadence Genus

Experience

Intel Corporation – Boxborough, MA

DFT Design Engineer June 2026 - Present

DFT Engineer working on pre and post Si areas. Areas include DFT synthesis insertion, Spyglass rules checking & analysis, ATPG pattern generation & coverage analysis, GLS & GLS debug on both untimed & timed setups, Si pattern miscompare analysis & vmin debug. Experience with both stuck-at & at-speed pattern generation and associated setup. Additionally responsible for reporting automation, pattern generation flow optimization, vendor relations, and provided mentorship to interns and junior team members.

Cadence Design Systems – Remote MA

Sr. Principal Design Engineer May 2025 – June 2026

Working as a DFT Engineer for Cadence's Palladium EPU (emulation processor unit). Aspects of role include: working on synthesis of subblocks and RTL level DFT insertion into given blocks, pattern generation and coverage analysis of chip subcomponents, assisting with DFT architecture of the ASIC, hierarchical test planning and migration, gate-level pattern simulation analysis and debug, inter-product task management & alignment, and advising junior team member / interns.

Intel Corporation – Hudson/Boxborough, MA

DFT Design Engineer November 2020 – May 2025

Cadence Design Systems – Endicott, NY

Lead Product Engineer June 2017 – November 2020

R&D Product Engineer for the Modus DFT Software Solution, supporting multiple parts of the system including but not limited to: ATPG, Hier Test, DFT, & LBIST. Responsibilities include: Debugging customer test issues, making demo parts for development team use, assisting in architecture of new features, conducting field education of customers and in-house team members, & documentation updates. Customers supported include global semiconductor companies and major defense contractors.

Syracuse University Dept. of Electrical Engineering & Computer Science

Teaching Assistant June 2014 – May 2017

Instructed Junior and Senior Computer Engineering Lab course students in methodology of design and usage of; FPGAs/CPLDs, microcontrollers, and Embedded Systems. Assisted in development of new lab course materials.

Education

Syracuse University, M.S. Computer Engineering June 2017
Syracuse University, B.S. Computer Engineering June 2015